module cond(clk,out,carryout,en\_ov,en\_zero);

input clk;

input carryout;

input [7:0]out;

output reg en\_ov=0,en\_zero=0;

reg w;

always@(posedge clk)

begin

w<=(out==8'b0);

case({w,carryout})

2'b00:begin en\_ov<=1'b0;en\_zero<=1'b0;end

2'b01:begin en\_ov<=1'b1;en\_zero<=1'b0;end

2'b10:begin en\_ov<=1'b0;en\_zero<=1'b1;end

2'b11:begin en\_ov<=1'b1;en\_zero<=1'b1;end

endcase

end

endmodule